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ISL9492 Quick Start Guide

1. Install the ISL9492 Evaluation Board Installer from Intersil's website ISL9492_eval_installer_1_0.exe. This program allows the USB bus to talk to Intersil's I^2C evaluation board, which communicates to the ISL9492 LNB board.
2. Install the ISL9492 USB I^2C Driver Installer - islusbi2c_driver_installer_1_0.exe. This program provides the GUI (graphical user interface) to control the various commands on the ISL9492 via I^2C.
3. After installing program, go to 'start' menu in Windows, 'all programs', 'Intersil', 'ISL9492', and select 'ISL9492 Eval'. The screen should look similar to Figure 1.
4. Go to Device Select and choose ISL9492 from the dropdown menu. The screen should look like Figure 2.

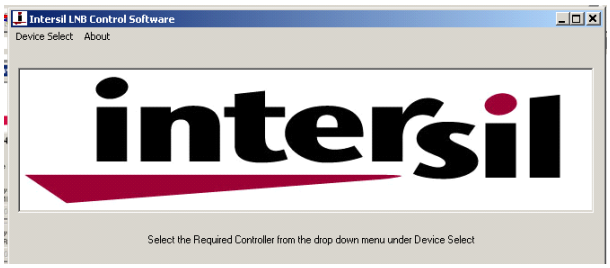

FIGURE 1. CONTROL SOFTWARE WINDOW

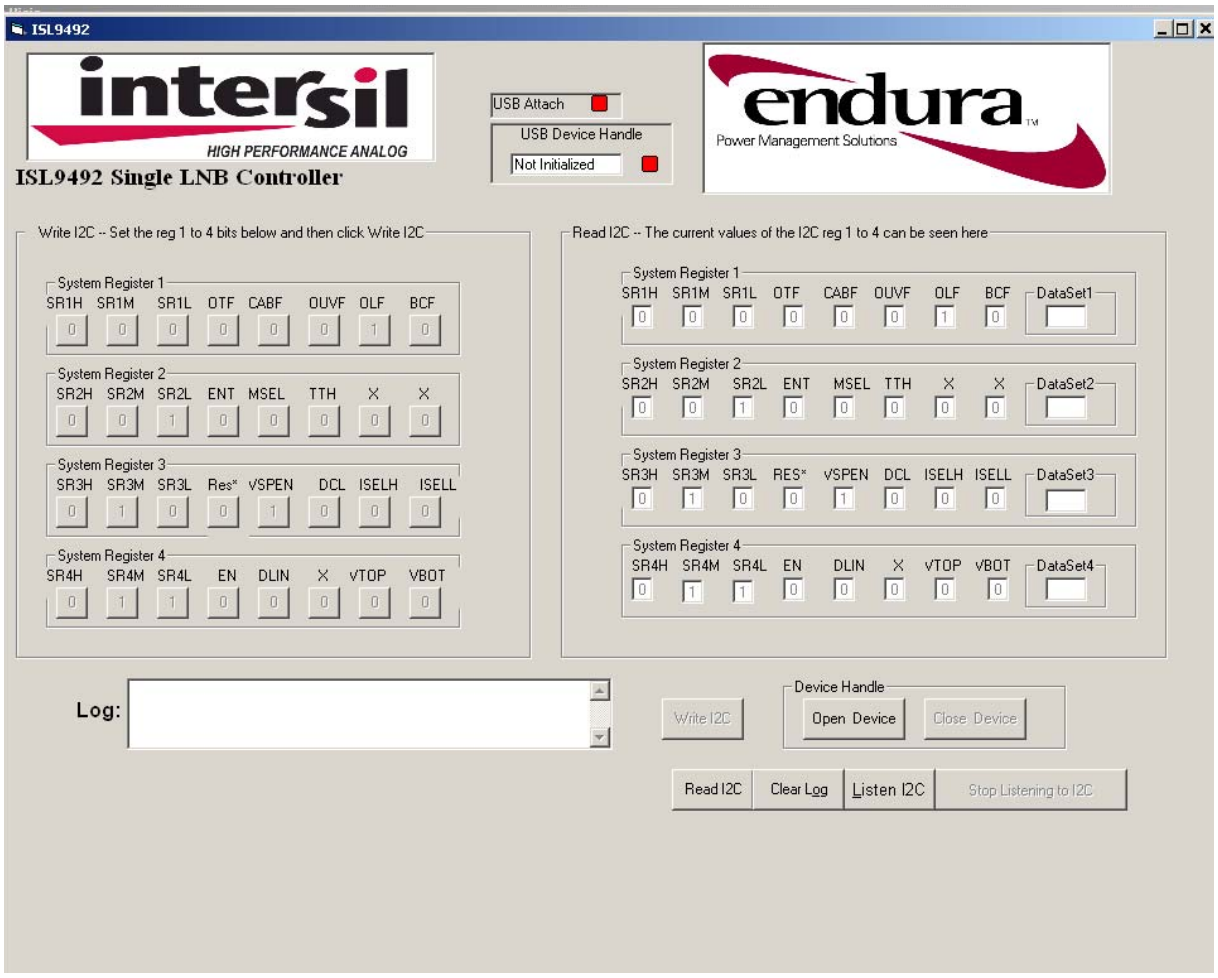

FIGURE 2. LNB CONTROLLER WINDOW

5. Apply a +12V supply to V_{CC} and GND to the Return post on the ISL9492QFNEVAL1 evaluation board. Connect a USB connector and one end of the 4-wire connector to the I^2C daughter board. The other end of the 4-wire connector goes to the ISL9492QFNEVAL1 evaluation board, jumper J1 as shown in Figure 3.

6. Choose 'Open Device' from the GUI. The "USB Attach" and "USB Device Handle" buttons should have turned green indicating that the GUI is communicating with the ISL9492QFNEVAL1 evaluation board.

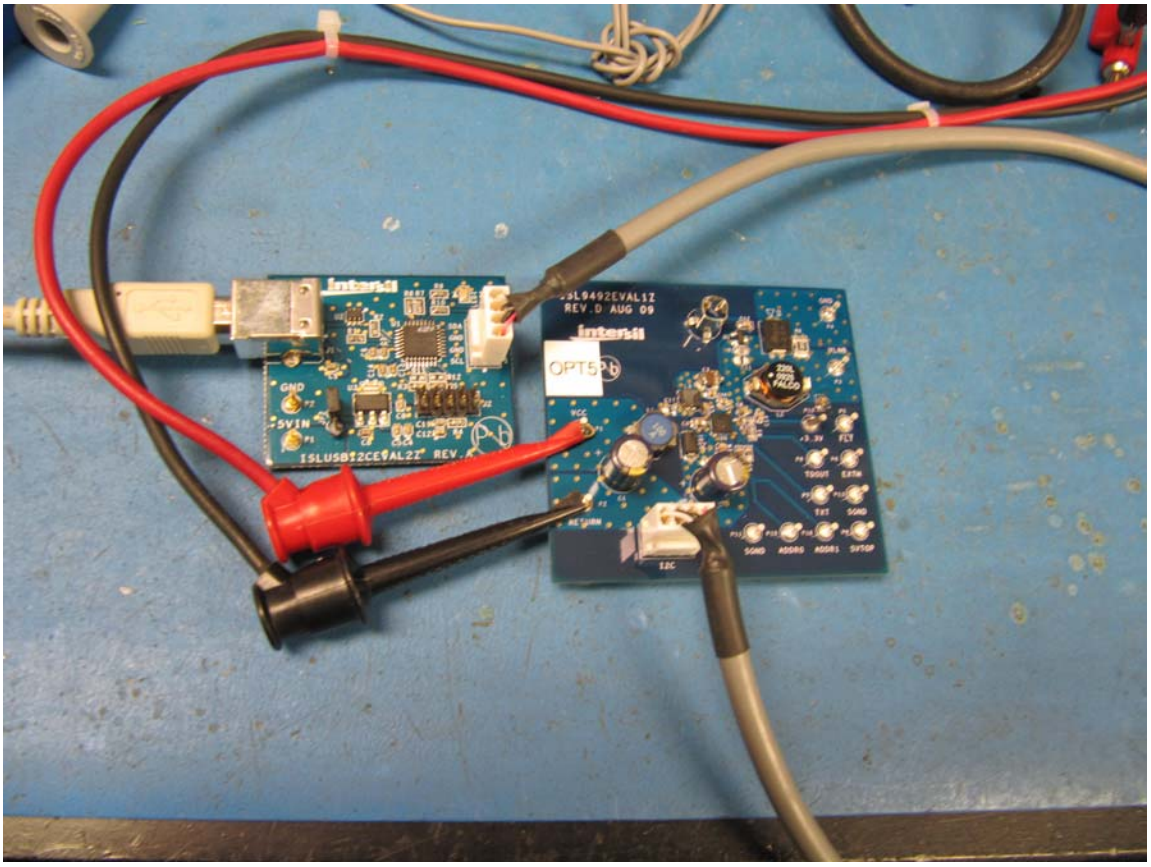

FIGURE 3. ISL9492QFNEVAL1 EVALUATION BOARD CONNECTION

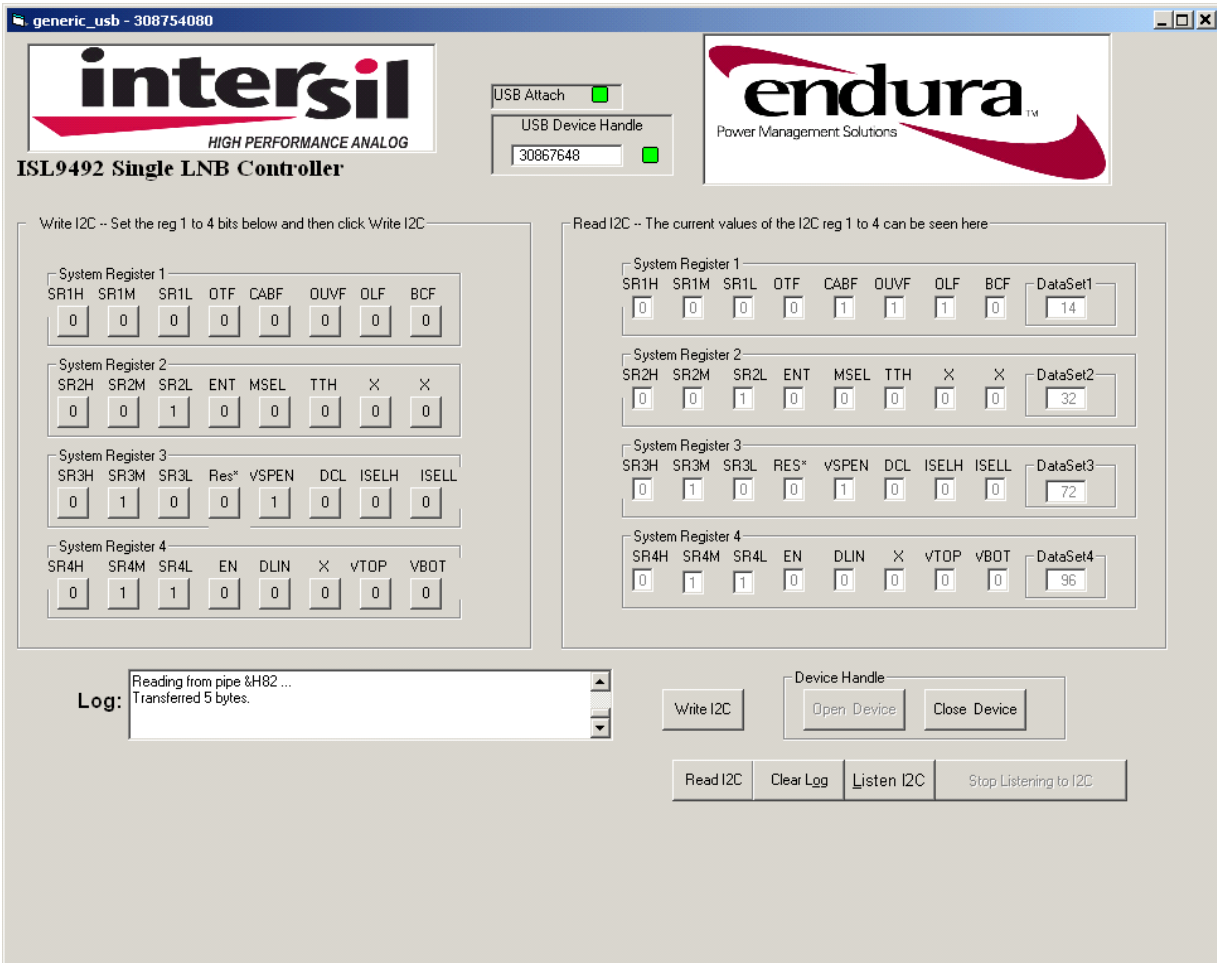

FIGURE 4. ISL9492 SINGLE LNB CONTROLLER

7. The green trace in Figure 5 shows the soft-start time of VLNB to be approximately 24ms after the EN and DLIN bits in register 4 were toggled high. For a comprehensive description of system registers and I^2C commands, please refer to the ISL9492 datasheet.

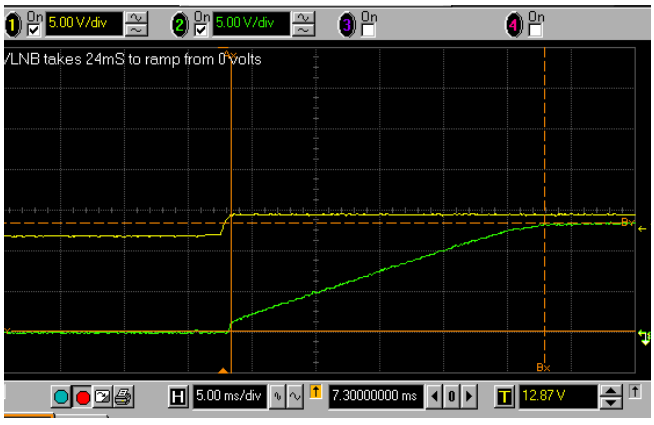

FIGURE 5. VLNB SOFT-START TIME

Figure 6 shows the 22kHz tone on VLNB output at 13.3V from $12V_{IN}$ with 700mA of resistive load current after ENT and TTH bits in register 2 are toggled high. Use of active load during this test is not recommended due to high input capacitance, which could potentially distort the output tone signal.

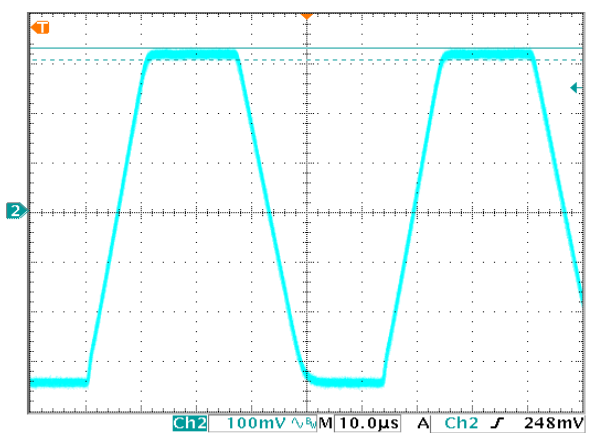

FIGURE 6. 22kHz VLNB OUTPUT AT 13.3V

ISL9492 Layout Guideline

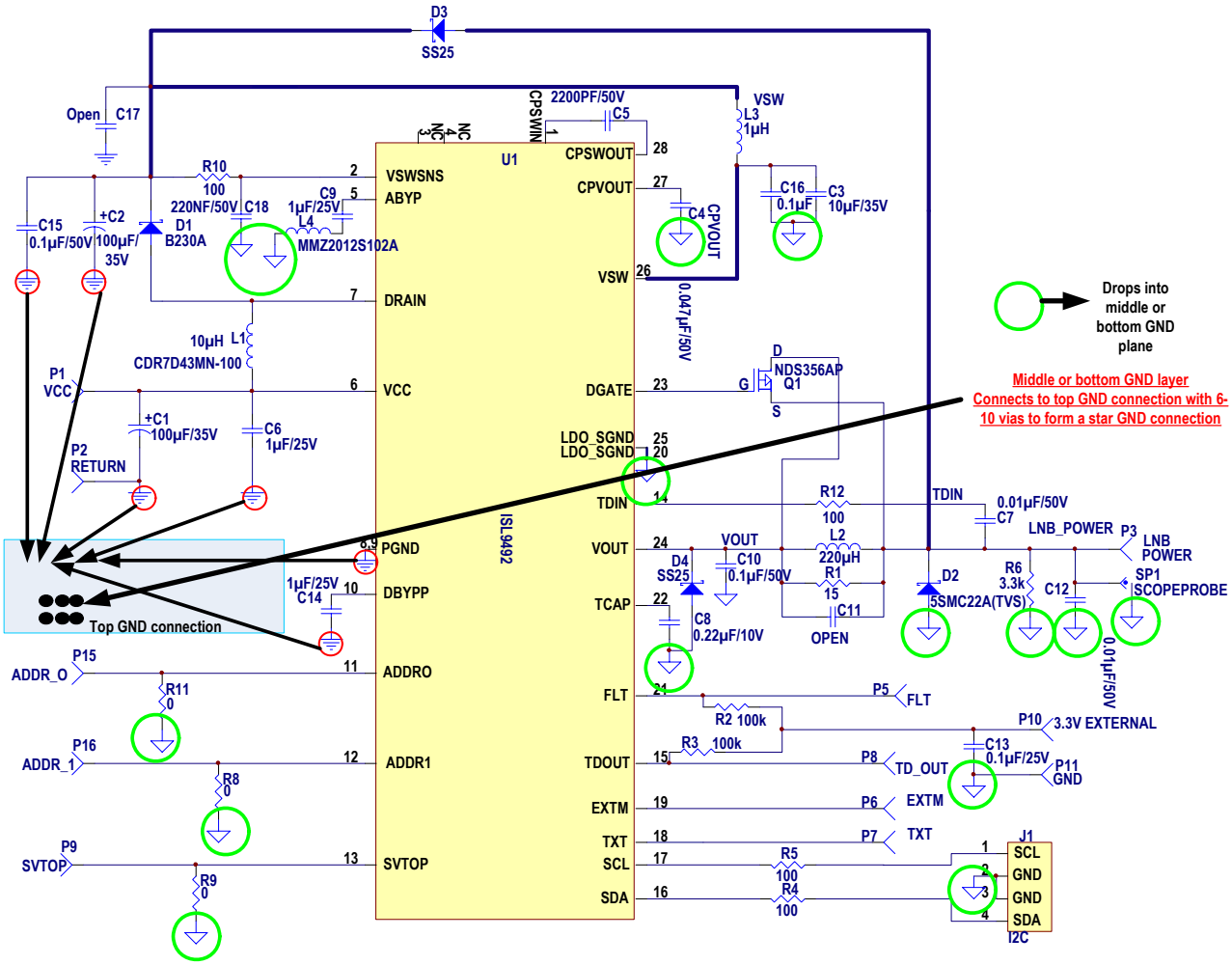

FIGURE 7. ISL9492 STAR GROUND CONNECTION ILLUSTRATION

It is highly recommended to connect GND of C1, C6, C14, C2, C15, pins 8 and 9 in a tight formation on the top layer as shown in red circles in Figure 7 and needs to be returned back to the input power supply GND post, which is on the bottom left of ISL9492 board . The ground side of the components in green circles along with the epad can be dropped to the internal ground plane which connects to the top ground plane with 8-10 vias near C1 to form a star ground connection.

Evaluation Board Schematic

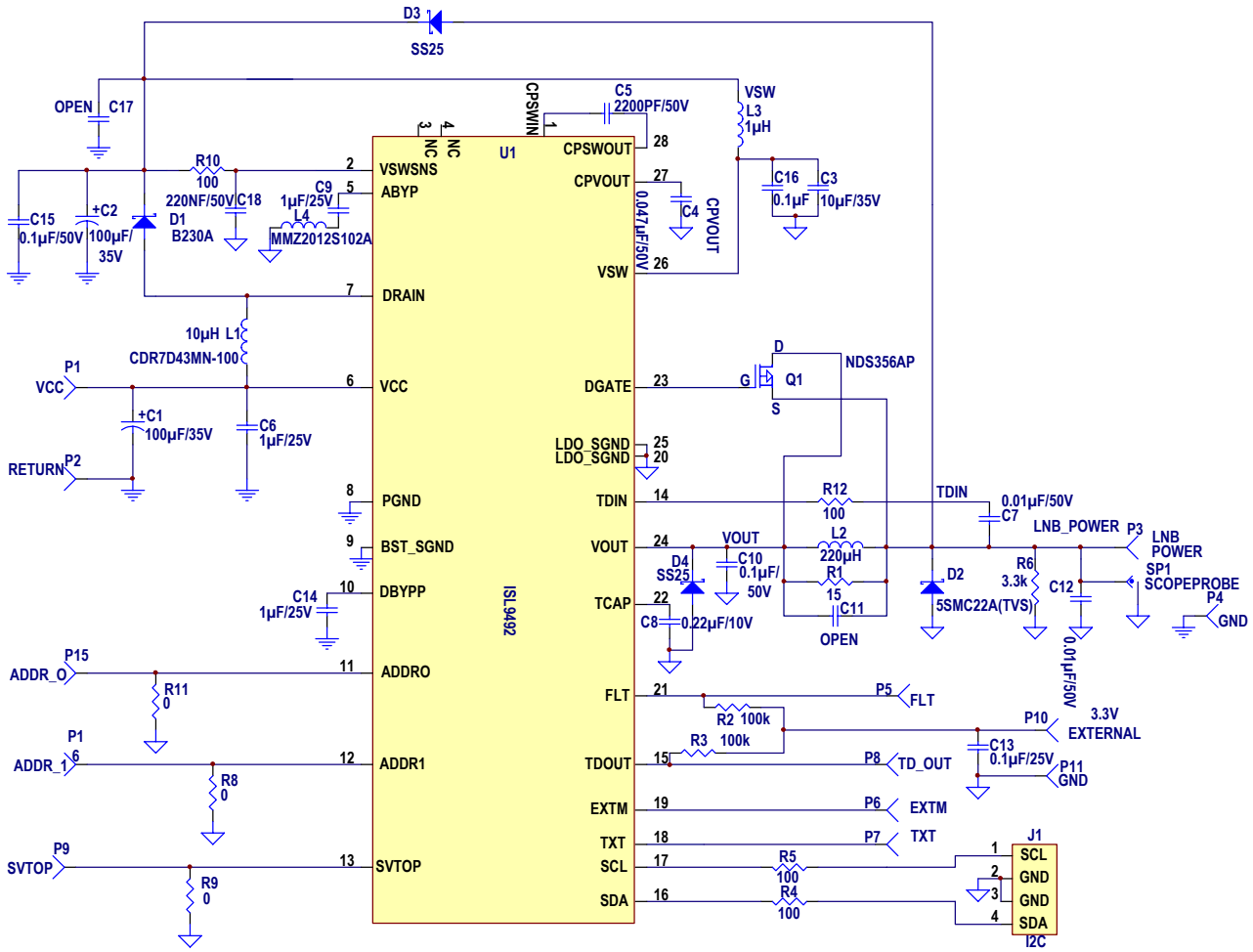

FIGURE 8. ISL9492QFNEVAL1 EVALUATION BOARD SCHEMATIC

Layout Guidelines

Since the ISL9492 has an integrated high power boost, careful attention has to be paid to the layout which are outlined as follows for a 4-layer and a 2-layer board:

1. Boost input capacitor (C1, C6), output boost capacitors (C2, C15), inductor (L1), Schottky diode D1 should be placed together in a nice tight layout. The ground connection of C1, C2, C15, C6, ISL9492 pins 8, 9 and C14 should go directly to the GND input supply as shown in Figure 9.
2. C3, C16 and C10 ground connection is returned directly to pin 25, LDO-SGND (see Figure 9). Ground connection of L4, C18, C8, C4, and pin 20, are dropped directly to an internal ground island (see Figure 10). This layer is connected to the ground plane at C1 ground connection.
3. D4 is connected directly across pins 23 and 25. D2 and VLNB return post are returned back to the internal ground island as described in point 2.
4. ISL9492's EPAD is connected to an internal ground plane. This ground plane is connected to the top layer with multiple vias right under C1 and C2 ground connection (see Figure 11).
5. The bottom layer is used to connect output power post to D3, which connects back to C2 (see Figure 12).
6. C1, C2, C15, C6 and pins 8 and 9 are in a tight configuration with GNDs connected to input power post GND. All other components going to GND are dropped directly to the second GND plane. The second layer is connected to the top GND layer right next to C1 ground connection as shown in Figures 13 and 14.

4 and 2 Layer Demo Board Layout Examples

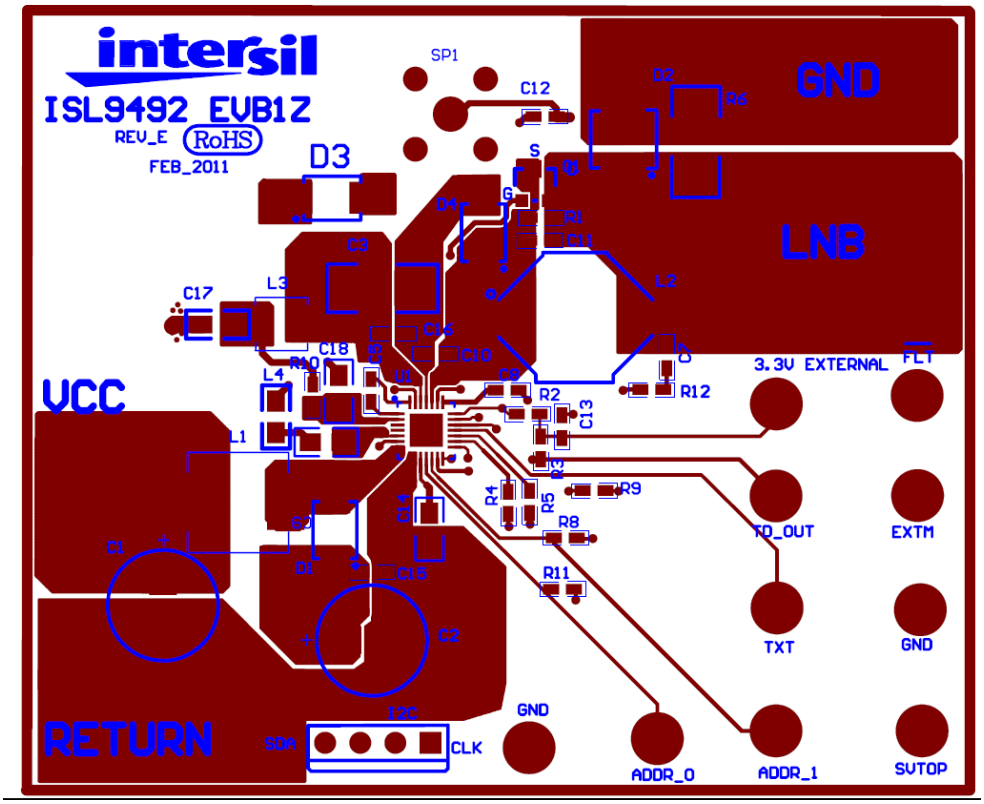

FIGURE 9. 4 LAYER - TOP

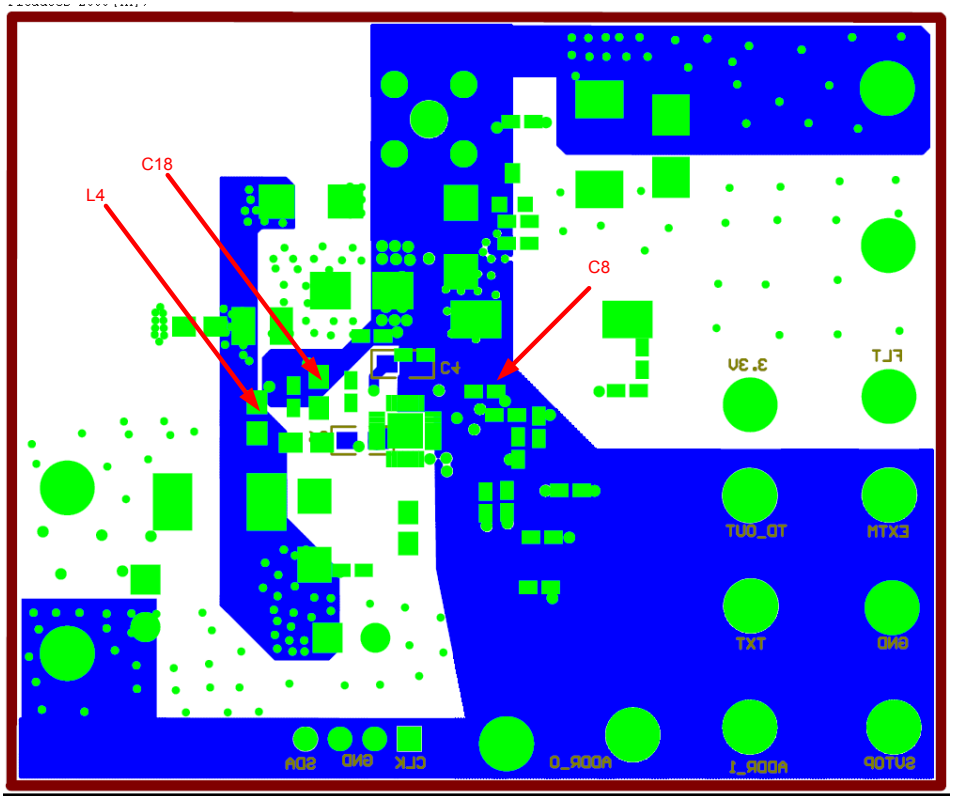

FIGURE 10. 4 LAYER - INNER GROUND

4 and 2 Layer Demo Board Layout Examples (Continued)

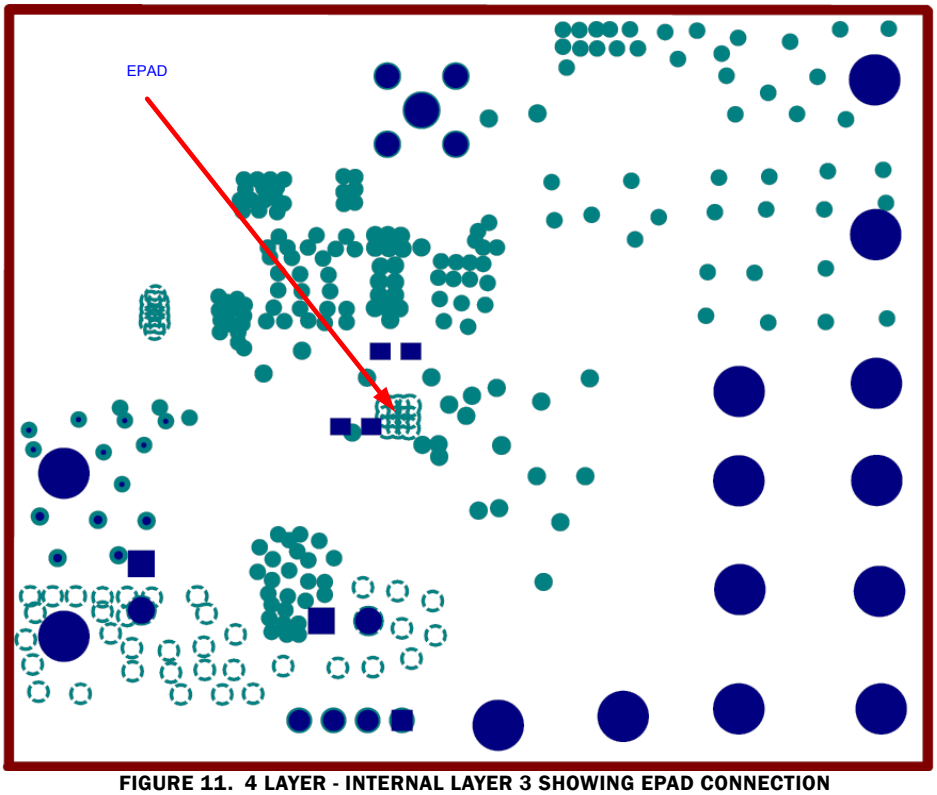

FIGURE 11. 4 LAYER - INTERNAL LAYER 3 SHOWING EPAD CONNECTION

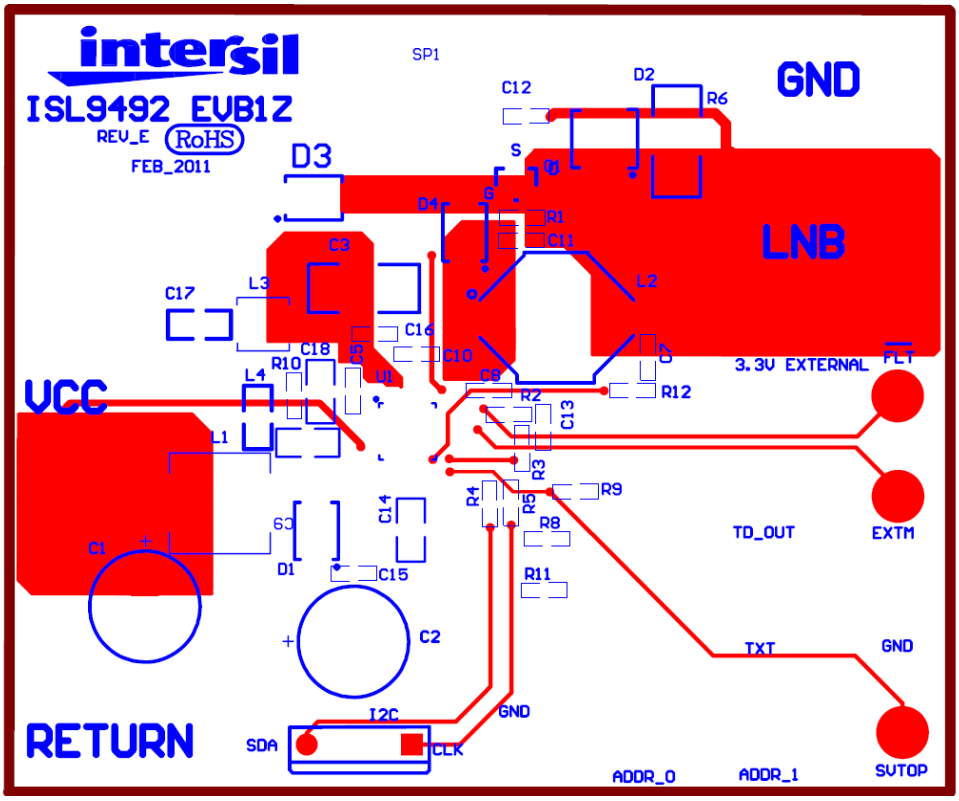

FIGURE 12. LAYER 4

4 and 2 Layer Demo Board Layout Examples (Continued)

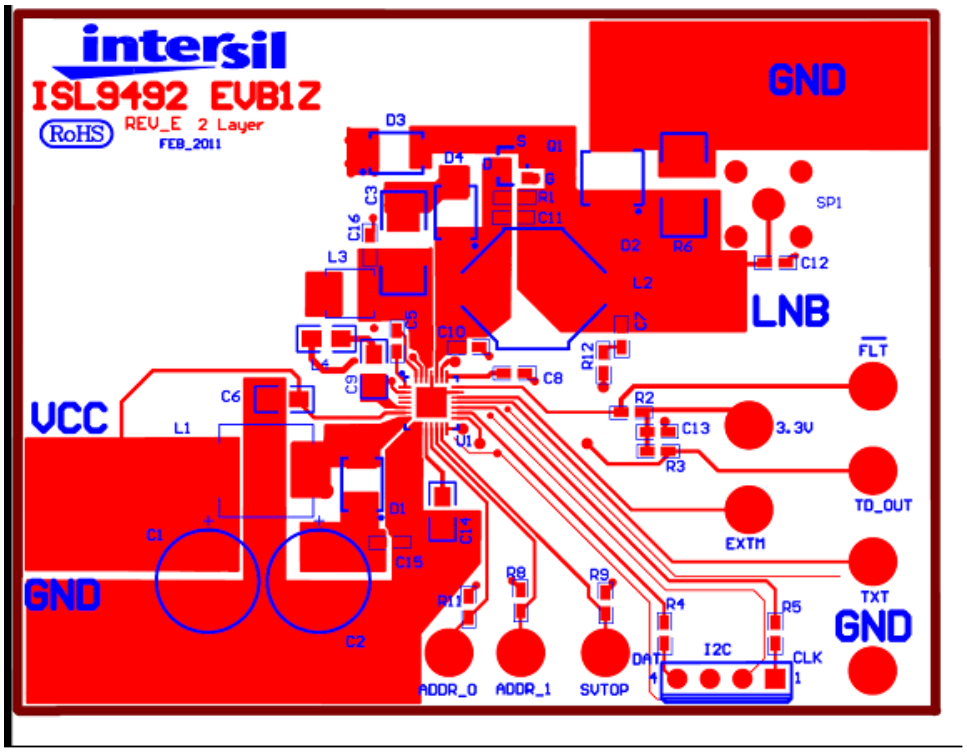

FIGURE 13. 2 LAYER - TOP

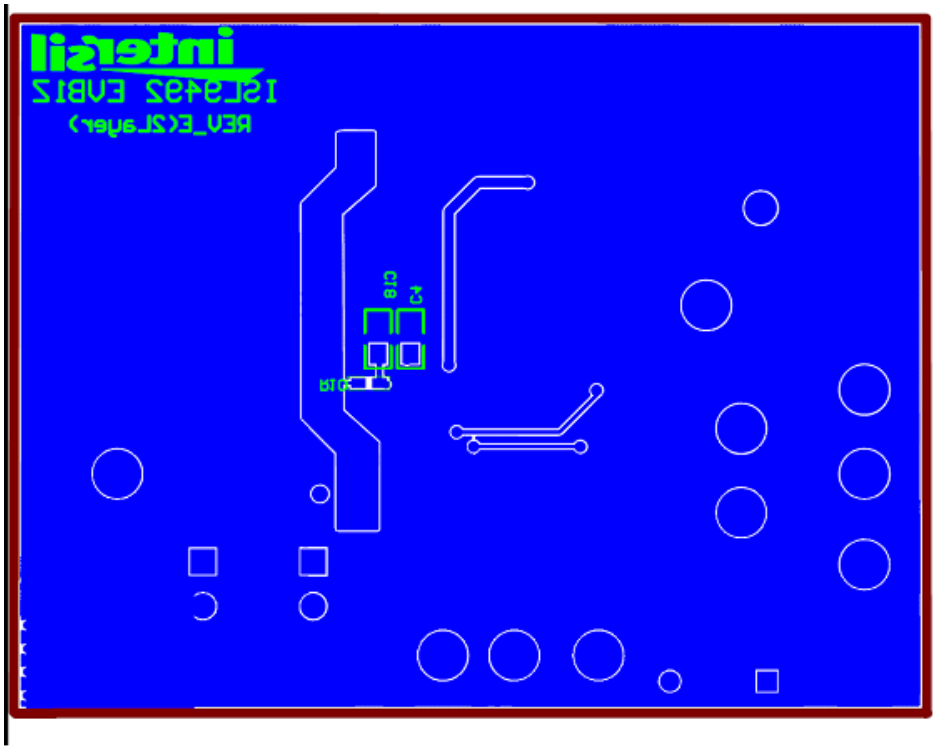

FIGURE 14. 2 LAYER - BOTTOM

ISL9492QFNEVAL1 Bill of Materials

PART TYPE	DESIGNATOR	FOOTPRINT
0.01µF/50V	C12	603
0.01µF/50V	C7	603
0.047µF/50V	C4	805
0.1µF/25V	C13	603
0.1µF/25V	C16	603
0.1µF/50V	C10	603
0.1µF/50V	C15	603
0.22µF/10V	C8	603
100µF/35V	C2	11.5x8 Aluminum
100µF/35V	C1	11.5x8 Aluminum
10µF/35V	C3	1210
10µH	L1	CDR7D43
1µF/25V	C14	805
1µF/25V	C6	805
1µF/25V	C9	805
1µH	L3	1008PS
2200PF/50V	C5	603
220NF/50V	C18	805
220µH	L2	DS3316
5SMC22A(TVS)	D2	DO-403A
B230A	D1	DO-214
LNB	P3	POWERPOST
MMZ1608S102AT	L4	603
NDS356AP	Q1	SOT-23
Open	C11	603
Open	C17	805
SS25	D3	DO-214
SS25	D4	DO-214
0	R11	603
0	R8	603
0	R9	603
15	R1	603
100	R10	603
100	R12	603
100	R4	603
100	R5	603
100k	R2	603
100k	R3	603
3.3k	R6	1210